Application Guidelines for Non Isolated Converters

AN04-008 Guidelines for Sequencing of Multiple Modules

Introduction

Today's electronics systems require multiple power supply voltages to power the various ICs. Board designers need to not just provide multiple voltages, but also to ensure proper voltage sequencing for each multi-voltage IC during power-up and power-down. The most common power supply architecture involves dual voltages; usually 1.8V or lower for the core power supply and 3.3V or 2.5V for supporting I/O.

Dual-voltage-supply architectures often need coordinated management of the core and I/O voltages during power-up and power-down, a requirement called sequencing.

In general, there are three types of power sequencing solutions that can be applied to provide a synchronized start-up and shutdown sequence of core and I/O voltages.

Sequential: The first method is called voltage cascading or sequential start-up where one of the voltages, often the core voltage, comes up first and reaches its final regulated value. After a certain specified delay, the other voltage is required to come up and reach its regulation value (see Figure 1). During power-down, the sequencing order of the supply voltages is reversed.

Ratiometric: A second sequencing solution is called the ratiometric approach, where both supply voltages reach the regulation point at the same time. In this scheme, the core and I/O voltages have different slew-rates, (see Figure 2) to enable both voltages to reach their regulation point at approximately the same time instant. During power-down using the ratiometric sequencing method, both output voltages start ramping down at the same time instant but with different slew-rates so that they reach zero at approximately the same time instant.

Simultaneous/Tracking: The third sequencing method is simultaneous start-up or voltage tracking where both voltages start ramping up with identical slew rates. After the core or lower voltage reaches its regulation level, the I/O voltage continues with the same slew-rate until it reaches its regulation voltage (see Figure 3). The pattern is reversed during the power-down sequence.

Using EZ-SEQUENCE™

All models of the DLynx™, TLynx™, Austin Lynx™ II series, and Austin MegaLynx™ are available with EZ-SEQUENCE™. This sequencing feature helps users implement any of the three types of the sequencing discussed above. The on/off control present in all modules can be used to turn them ON and OFF in a desired sequence using an external controller, and is generally employed in implementing the sequential method of sequencing. For implementing the ratiometric or simultaneous/tracking methods of sequencing more precise control of the timing and slope of the output voltage during start-up and shutdown is needed. This function is implemented through an additional pin called SEQ. When a voltage is applied to the SEQ pin, the output voltage tracks this voltage on a one-to-one basis until the output reaches the set-point voltage. This allows the output voltage to be brought up in a controlled manner as long as the final value of the SEQ voltage is made higher than the set-point voltage of the module.

By connecting the SEQ pins of multiple modules together, all modules track their output voltages to the voltage applied on the SEQ pin. When sequencing is not required in the application, the SEQ pin can either be tied to VIN or left unconnected and the module will turn-on with a delay and rise time as indicated in the product data sheets. Note that the following descriptions apply to all modules except the DLynx™ series. For the DLynx™ series, please refer to separate descriptions provided later in this application note.

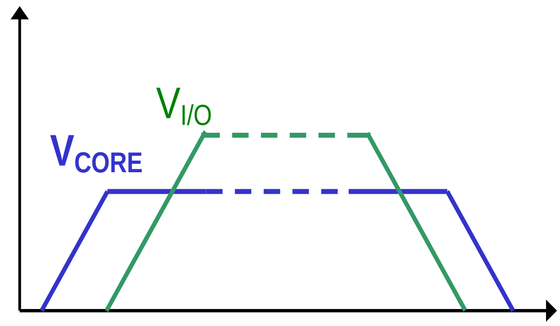

Figure 1. Voltage waveforms for sequential sequencing.

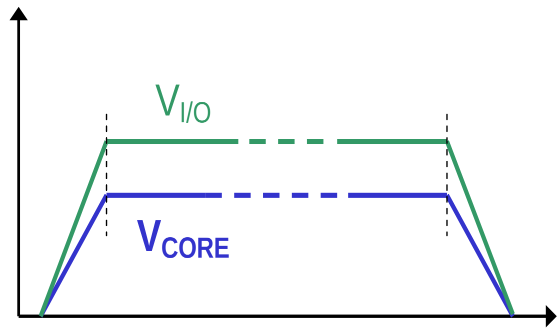

Figure 2. Voltage waveforms for ratiometric sequencing.

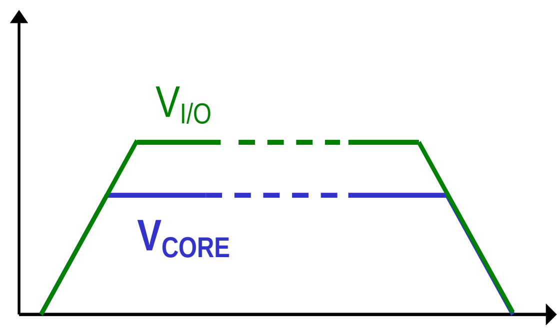

Figure 3. Voltage waveforms for simultaneous sequencing.

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General Design Considerations:

- For proper voltage sequencing, first, input voltage is applied to the module.
- The On/Off pin of the module is left unconnected (or tied to GND for negative logic modules or tied to VIN for positive logic modules) so that the module is ON by default.
- After applying the input voltage to the module, a delay of 10msec minimum is required before applying voltage on the SEQ pin. This delay gives the module enough time to complete its internal power-up soft-start cycle.
- During this delay time, the SEQ pin should be held close to ground, nominally 50mV (+/- 20mV). This is required to keep the internal op-amp out of saturation thus preventing output overshoot during the start of the sequencing ramp.
- By selecting R_{IN} (See Fig 4) according to the following equations, the SEQ pin voltage is at 50mV when the SEQ Control Voltage signal is zero:

For the TLynx series, $R_{pull\text{-}up}$=499kΩ

$$R_{IN} = 24{,}950 / (V_{IN}-0.05)$$

For the 5V Austin LynxII series, $R_{pull\text{-}up}$=400kΩ

$$R_{IN} = 20{,}000 / (V_{IN}-0.05)$$

For the 12V Austin LynxII series, $R_{pull\text{-}up}$=1MΩ

$$R_{IN} = 50{,}000 / (V_{IN}-0.05)$$

For the Austin MegaLynx series, $R_{pull\text{-}up}$=3MΩ

- R_{IN} = 150,000 / (V_{IN}-0.05) In case of multiple modules fed off a common sequencing control signal, each module needs a resistor (R_{IN}) connected to it's sequencing pin, SEQ or an equivalent single resistor R2 (defined below) that is connected to all SEQ pins tied together.
- After the 10msec delay, the voltage applied to the SEQ pin is allowed to vary and the output voltage of the module will track this voltage on a one-to-one volt basis until the output reaches the set-point voltage.
- In case of multiple modules fed off a common sequencing control signal, each module needs a resistor (R_{IN}) connected to it's sequencing pin, SEQ or an equivalent single resistor R2 (defined later) that is connected to all SEQ pins tied together.

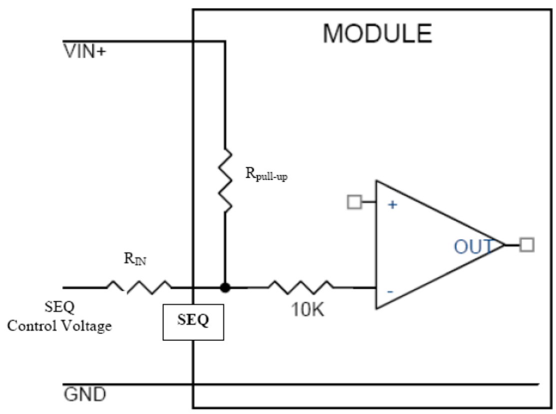

Figure 4. Sequencing signal interface of a module.

- To initiate simultaneous shutdown of the modules, the sequence pin voltage is lowered in a controlled manner. The output voltages of the modules track the sequence pin voltage when it falls below their set-point voltages.
- A valid input voltage must be maintained until the tracking and output voltages reach zero to ensure a controlled shutdown of the modules.
- The voltage on the SEQ pin can be obtained from a dedicated controller, the output of another module or from an RC circuit.
- The maximum sequencing voltage that can be applied to the SEQ pin is the maximum input voltage rating of the module(s).
- The module's output(s) can track the SEQ pin signal to within 100mV of voltage differential with slopes of up to 2V/msec during power-up and 1V/msec during power-down. For DLynx modules the allowable slope is only 0.5V/msec during power-up or power-down. However, during power down, since the sequencing control op-amp is in saturation, there is a slight lag of the output(s) from the sequencing signal prior to the start of the power down. This differential can be up to 200mV for about 200µsec. This is shown below in Fig 5. In case this is undesirable, even slower (approximately < 0.25V/ms) ramp down slope will be needed.

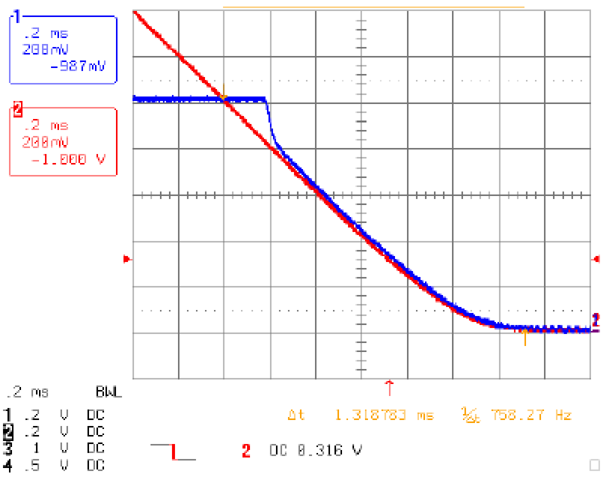

Figure 5. Power-down behaviour of the output (blue) with sequencing signal (red) with slew rate of 1V/ msec.

Typical Application 1: Simultaneous start-up of multiple modules with an input voltage, V_{IN} as a common sequencing control voltage.

Simultaneous sequencing of multiple modules can be implemented using the circuit configuration shown in Fig 6. The circuit works by providing the same control voltage as V_{IN}. In general, this control voltage can be provided from any source.

First, input voltage is applied to the modules. Transistor Q1 is turned on before V_{IN} reaches the minimum input voltage threshold of the modules. Resistor R2 (equivalent sequencing resistor) is selected to maintain nominal 50mV on the SEQ pins until the voltage on the SEQ pin starts to rise (after a minimum

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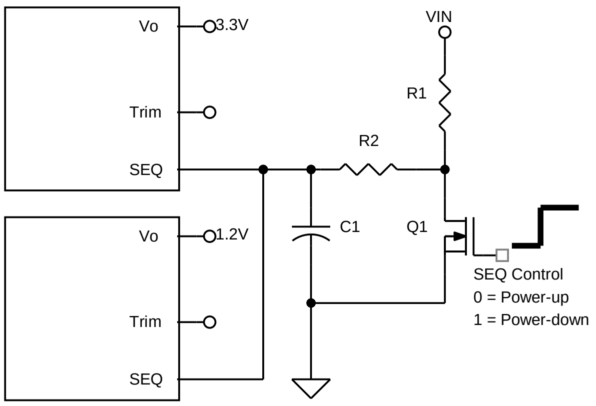

Figure 6. Circuit configuration for simultaneous sequencing.

of 10ms delay from when input voltage is applied to the modules).

The equations for calculating R2 to maintain 50mV at the SEQ pin are given below for multiple modules (where N is the number of sequenced modules):

$$R2 = \frac{24{,}950}{N(Vin,\min - 0.05)}$$ (TLynx series)

$$R2 = \frac{20{,}000}{N(Vin,\min - 0.05)}$$ (5V Austin LynxII series)

$$R2 = \frac{50{,}000}{N(Vin,\min - 0.05)}$$ (12V Austin LynxII series)

$$R2 = \frac{150{,}000}{N(Vin,\min - 0.05)}$$ (Austin MegaLynx series)

Table 1 provides the required values of R2 to maintain 50mV on the SEQ pin for various input voltages and number of modules used for sequencing for the Austin Lynx II series.

To initiate shutdown, Q1 is turned back ON, and this starts the discharge of capacitor C1 through R2. As the voltage on the SEQ pins falls, the output voltages of the modules also fall, with the higher output voltage module starting its output voltage descent first.

Table 1 (Lynx II Series)

Bus Voltage (V_{IN})	Resistor R2 (kΩ)	No of Modules (N)
3.3V	3.4	2
5V	2.2	2
12V	3.03	2
3.3V	2.3	3
5V	1.5	3
12V	2.02	3

The corresponding scope plots describing the power-up and power-down sequences are shown in Figures 7 and 8 respectively. The slope of the voltage on the SEQ pin can be set by selecting values for R1, R2 and C1.

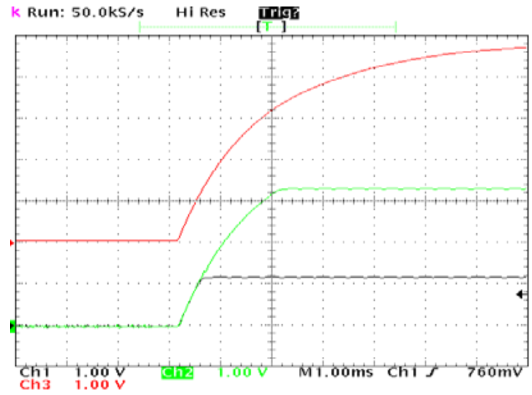

Figure 7. Scope plots showing simultaneous start-up waveforms. The upper waveform is the voltage at the SEQ pin, and the lower waveforms are the two output voltages.

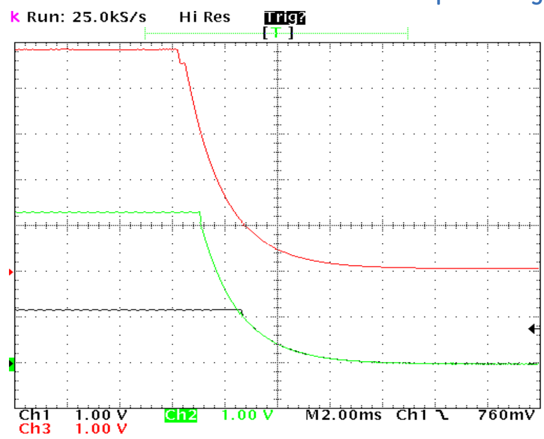

Figure 8. Scope plots showing simultaneous power-down waveforms. The SEQ pin waveform is the upper one, and the two output voltages are the lower waveforms.

Table 2 shows typical values of R1, R2 and C1 for various slopes of power-up and power-down sequencing for the 5V Austin Lynx II series.

Table 2 (For 5Vin Lynx II Series)

VIN V	R1 kΩ	R2 KΩ	C2 µF	dV/dt (V/msec) Power-Up	dV/dt (V/msec) Power-Down
5.0	1.0	2.2	10	0.1	0.06
5.0	1.0	2.2	4.7	0.25	0.14
5.0	1.0	2.2	2.2	0.5	0.25
5.0	1.0	2.2	1.5	0.75	0.4
5.0	1.0	2.2	1.0	1.0	0.5

Typical Application 2: Simultaneous start-up of multiple modules with sequence control voltage derived from the module with the highest output voltage.

One of the most common circuit configurations for simultaneous start-up of multiple modules uses the highest voltage output module as the control voltage on the SEQ pin of the other modules. This ensures that all the outputs track the

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highest voltage till their set-point voltage. Figure 9 shows the circuit configuration with simultaneous start up using this approach. The circuit comprises of three non-isolated 12V input T-Lynx modules (APTS003A0X) with outputs trimmed (Trim resistors not shown) to 5V, 3.3V and 2.5V. All three modules are –ve enable (i.e. -ve On/Off logic) modules.

Typical Application 2: Simultaneous start-up of multiple modules with sequence control voltage derived from the module with the highest output voltage.

One of the most common circuit configurations for simultaneous start-up of multiple modules uses the highest voltage output module as the control voltage on the SEQ pin of the other modules. This ensures that all the outputs track the highest voltage till their set-point voltage. Figure 9 shows the circuit configuration with simultaneous start up using this approach. The circuit comprises of three non-isolated 12V input T-Lynx modules (APTS003A0X) with outputs trimmed (Trim resistors not shown) to 5V, 3.3V and 2.5V. All three modules are –ve enable (i.e. -ve On/Off logic) modules.

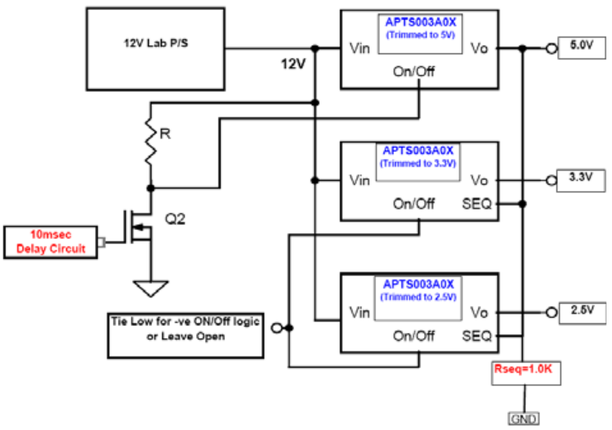

Figure 9. Circuit configuration for an example for simultaneous start-up of three modules.

To achieve simultaneous start up of these modules, the output of the highest output module (5V) is used as the tracking voltage and is consequently tied to the SEQ pins of the other two modules. The On/Off pins of the lower output (3.3V and 2.5V) modules are tied to ground or left open to keep the modules on by default as the output of these modules are now controlled through the SEQ pin. First, the input to the non-isolated modules is applied by turning on the 12V supply. The 5V module is initially kept off by keeping Q2 off and pulling its On/Off pin high via resistor R connected to the input voltage. Since the 5V module's output is tied to the SEQ pin of the other two modules, their outputs will be close to ground (actually 50mV due to the presence of the equivalent sequencing resistor, Rseq=1.0K; this is the same as equivalent sequencing resistor R2 for N=2 defined earlier). Alternately, in order to meet the 50mV requirement prior to start-up, each of the two module's (3.3V and 2.5V) sequencing pin can be individually tied with 2.1K resistor to ground (this is the same value as R_{IN} calculated per module).

Assigning an individual sequencing resistor per module may be useful for creating standard designs when different families (e.g. a mixture of LynxII and TLynx) of the modules are required. This results in a less cumbersome design than trying to find the parallel combination of all the modules with a single resistor.

After a pre-set delay (10ms minimum), Q2 is turned on which turns on the 5V module. The two lower output modules will now track the 5V rail as shown in Fig. 10.

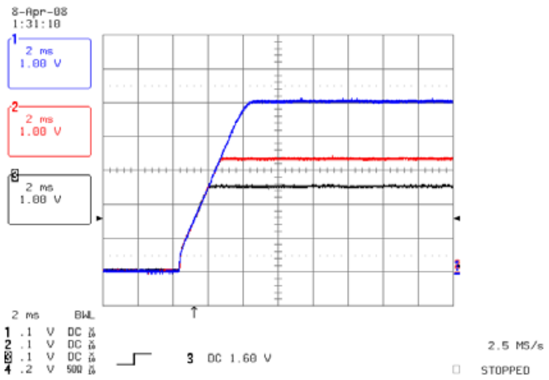

Figure 10. Scope plot showing output voltage waveforms during the simultaneous power-up of multiple modules for the circuit of Fig 9.

Ratiometric Start-up

Ratiometric start-up is achieved by applying control voltages proportional to the respective nominal output voltages to the SEQ pins of the two modules. These proportional voltages on the SEQ pins will result in two different output slew-rates, with each module reaching its set-point voltage at approximately the same time instant. Figure 11 shows the circuit configuration with proportional control voltages applied to each of the two modules. Figure 12 shows the ratiometric start-up sequence with control voltages on the SEQ pins and the resulting output voltages with identical rise times. Figure 13 shows the power down sequence with this configuration.

Values of R3 and R4 for desired output voltages can be determined by the following equation:

$$\frac{V2}{V1} = \frac{R4}{R3 + R4}$$

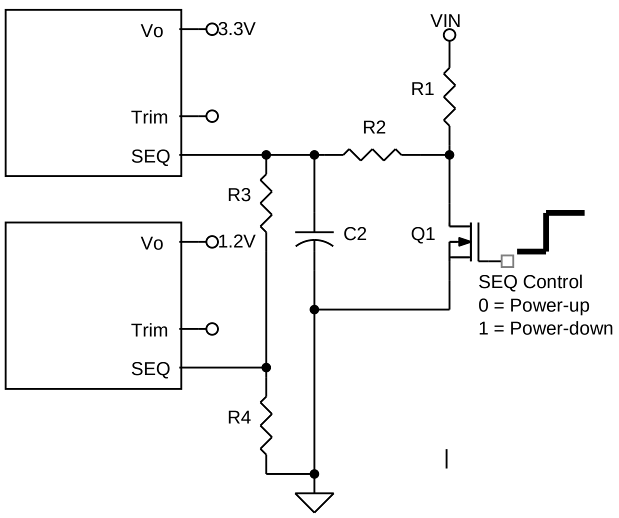

Figure 11. Circuit configuration for ratiometric sequencing.

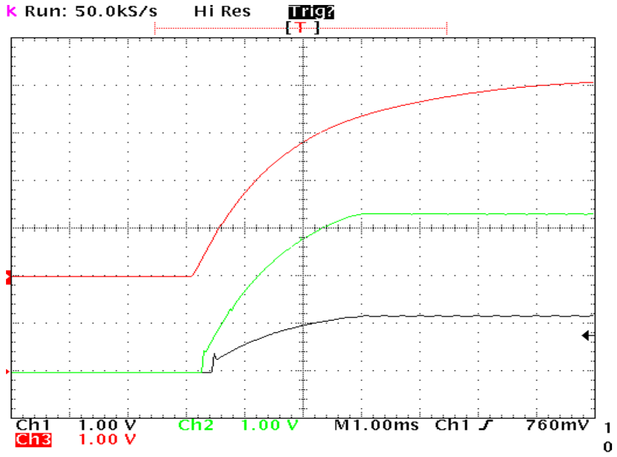

Figure 12. Scope plot showing the ratiometric start-up of two modules. Upper waveform shows the tracking voltage while the two lower waveforms are the output voltages.

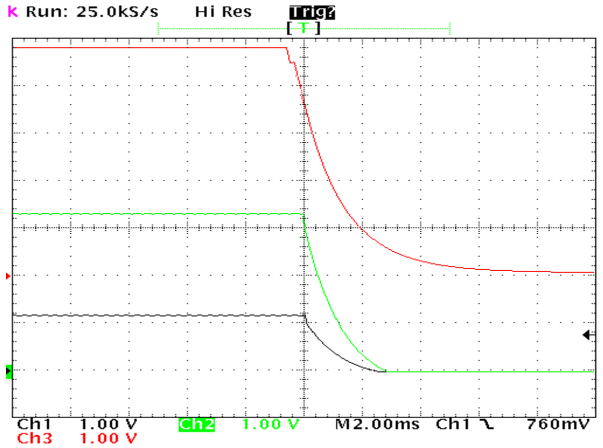

Figure 13. Scope plot showing the ratiometric power-down sequence of two modules. Upper waveform shows the tracking voltage while the two lower waveforms are the output voltages.

Sequential Start-up

Sequential start-up can be implemented easily using the on/off pin alone and does not require using the SEQ pin. The **Application Note AN004-03** ***titled "Application Guidelines for Non-Isolated Converters – On/off Considerations"*** provides guidelines and an example for how sequential start-up can be implemented.

Sequencing with the Digital DLynx™ Series

The Digital DLynx™ series of modules have a different set of requirements to implement sequencing. The main difference is that the sequencing voltage applied to the SEQ pin on these modules needs to be divided down by the same ratio used to divide down the output voltage using the Rtrim resistor. As shown in Figure 14, this can be accomplished by using a divider network with a 20KΩ upper resistor and a lower resistor equal to the Rtrim resistor (used to set the output voltage of the module). In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

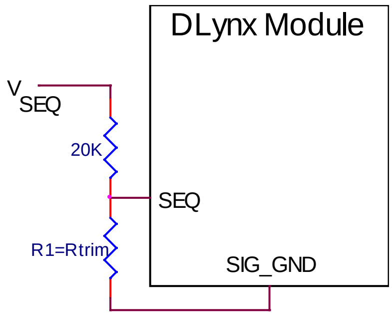

Figure 14. Circuit showing connection of the sequencing signal to the SEQ pin.

For DLynx™ modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up. Note that there is no requirement that the SEQ input be kept at 50mV before the module is turned ON.

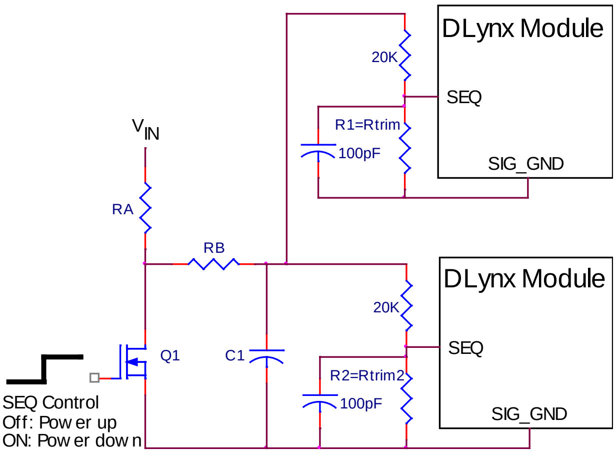

Figure 15. Circuit configuration for simultaneous sequencing of DLynx™ modules.

The data sheets for the DLynx™ modules indicate the maximum slew rates that can be used when the output voltage is being ramped up and down. These limits must be adhered to in order to ensure proper operation of the modules. Excessively large slew rates can cause damage to the modules under certain circumstances.

Note that in all DLynx™ series modules, the PMBus Output Undervoltage Fault will be tripped when sequencing is employed. This will be detected using the STATUS_WORD and STATUS_VOUT PMBus commands. In addition, the SMBALERT# signal will be asserted low as occurs for all faults and warnings. To avoid the module shutting down due to the Output Undervoltage Fault, the module must be set to continue operation without interruption as the response to this fault (see the description of the PMBus command VOUT_UV_FAULT_RESPONSE for additional information).

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Typical Application 3: Simultaneous start-up of multiple DLYNXTM modules with an input voltage, V_{IN} as a common sequencing control voltage.

Figure 15 shows the schematic diagram of a setup where two DLynxTM modules are set up to be controlled by the same sequencing voltage which is derived from V_{IN}. Transistor Q1 is turned ON before V_{IN} reaches the turn-on threshold of the modules. To initiate ramp up of the sequencing voltage, Q1 is turned OFF. To illustrate the design of a circuit such as the one shown in Figure 15, an example will be used. The two DLynx modules are operated with V_{IN} = 12V and set for outputs of 3.3V (upper module) and 1.2V (lower module) respectively. This sets R1 = 4.444KΩ and R2=20KΩ.

For the max allowed ramp up rate (dV/dt) on the output voltages of 0.5V/ms, the initial rate of rise of the voltage on C1 also needs to be 0.5V/ms (this corresponds to the rate when Q1 is turned OFF). Since the voltage on C1 will rise exponentially when Q1 is turned OFF, the highest rate of rise will be at the instant that Q1 is turned OFF. The rate of rise of the voltage on C1 is given by

$$\frac{dV_{C1}}{dt} = \frac{i_{C1}}{C1} = \frac{V_{IN}}{C1 \times RA}$$

The final value of the voltage on C1 is based on the resistor network connected between V_{IN} and the SEQ pins of the modules and ground. The resistance between V_{IN} and C1 is RA + RB, while the resistor across C1 is the parallel combination of the each of the 20K resistors and the corresponding resistors equal to RTrim for the module. In this particular example, the total effective resistance in parallel with C1 is the parallel combination of (20KΩ + 4.444KΩ) and (20KΩ + 20KΩ) or 15.172KΩ.

The resistors RA and RB need to be selected so that the final voltage across C1 is larger than the highest output voltage of the modules being sequenced. Resistor RB is usually selected as a small value - 100Ω is a recommended value. A suitable value for RA is to then make it approximately equal to the parallel resistance across C1 and so a value of 15KΩ for RA is selected in this example.

With RA+RB equal to 15.1KΩ, the capacitor C1 can be sized to obtain the initial dV/dt of 0.1V/ms using the following equation:

$$C1 = \frac{V_{IN}}{\frac{dV_{C1}}{dt} \times (RA + RB)}$$

In this example, this yields a value for C1 of 1.6μF.

Figure 16 shows simulated waveforms of the voltage on capacitor C1 and the output voltages of the two modules in the example discussed here. They show that the outputs of the module track the sequencing voltage (across C1) until the set output voltage level is reached, after which the module output remains there.

Similar circuits can be used for ratiometric startup and shutdown as well as long as the voltages are divided down appropriately to the various modules.

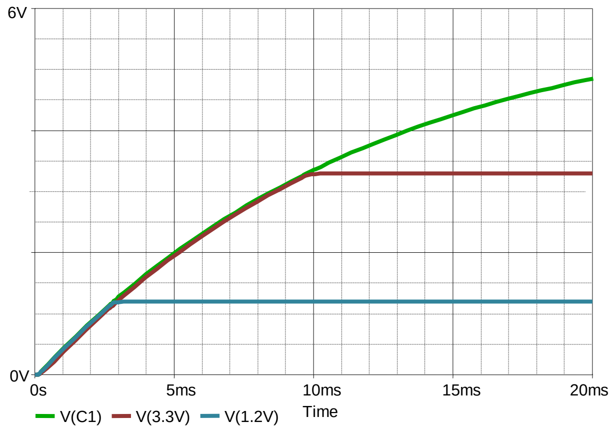

Figure 16. Simulated waveforms for the circuit of Figure 15 showing how the module output voltages track the sequencing voltage.

Summary

The EZ-SEQUENCE feature in the DLynxTM, TLynxTM, Austin LynxTM II and Austin MegaLynxTM series of modules provides the extra level of flexibility needed to power loads that require a precise sequence of voltages during the power up and down phases. By use of the sequencing pin and the example circuits shown in this application note, all three types of sequencing – sequential, tracking/simultaneous and ratiometric can be supported.

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